## REMARKS

Claims 1-10 are pending. Claim 1 has been amended. No new matter has been added by way of this amendment. Reconsideration of the application is respectfully requested.

Claims 1 and 3-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,229,513 to *Nakano* et al., while claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the same reference in view of U.S. Patent No. 6,404,533 to *Fergusson*. This rejection is respectfully traversed.

Claim 1 recites "an input interface for receiving plural types of video signals, adapted to select a first-type video signal from the plural types of video signals and generate a first digital video signal according to the first-type video signal."

U.S. Patent No. 6,229,513 to *Nakano* et al. relates to techniques for use in a liquid crystal display apparatus for lowering the frequency of clock signals that are sent to driving devices. According to this patent, this is accomplished by using driving devices that are similar to those encountered in conventional liquid crystal display apparatuses, without increasing the bus width of a bus line for transmitting the display data therethrough (see col. 2, lines 61-67). However, this patent fails to teach the limitation of "an input interface for receiving plural types of video signals, adapted to select a first-type video signal from the plural types of video signals and generate a first digital video signal according to the first-type video signal," as set forth in claim 1.

According to col. 5, lines 4-8 of the *Nakano* et al. patent, however, the receiver 160 converts the serial signal to the original parallel signals, and sends the recovered display timing signal DTMG, horizontal synchronization signal Hsync, vertical synchronization signal Vsync and display data (R, G, B) to the display control unit 110. Accordingly, Applicants respectfully assert that the receiver 160 as set forth in the *Nakano* et al. patent is not equivalent to the input interface set forth in claim 1.

Secondly, claim 1 recites the limitation "a scaler module, comprising a time control unit, and is provided to receive the first digital video signal." In contrast, the *Nakano* et al. patent only discloses a D-type flip-flop 111 that divides the clock signal CK at 65 MHz into D4 and D5 at 32.5 MHz (see col. 6, line 64 to col. 7, line 2). The *Nakano* et al. patent simply fails to teach the scaler module, as set forth in claim 1. As a result, the D-type flip-flop 111 in *Nakano*'s patent is not equivalent to the scaler module set forth and claimed.

On page 2 of the Office Action, the statement is made that :

> "Nakano differs from claim 1 in that he does not specifically teach a micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal. However, it would have been obvious to obtain the micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal in order to provide ability of fetch, decode, and execute instructions and to transfer information to the display device."

In response to the above statement, Applicants respectfully assert that the Examiner has failed to provide a specific teaching of a micro-processor as disclosed, set forth, and claimed in Applicants' claim 1. Hence, Applicants respectfully assert that the Examiner

has failed to establish a *prima facie* case of obviousness with respect to claim 1. Therefore, it is Applicants' belief that *Nakano* et al. fails to teach or suggest the use of "a control board integrating the input interface, the scaler module and the micro-processing device together," as disclosed in claim 1.

U.S. Patent No. 6,404,533 to *Fergusson* relates to an optical amplitude modulator for modulating signals for transmission by a fibre optic link (see col. 2, lines 30-33). However, this reference also fails to teach the specific limitations set forth in claim 1, and thus fails to cure the deficiency of the *Nakano* et al. patent. Specifically, *Fergusson* fails to teach the limitations of "an input interface for receiving plural types of video signals, adapted to select a first-type video signal from the plural types of video signals and generate a first digital video signal according to the first-type video signal" and "a scaler module, comprising a time control unit, and is provided to receive the first digital video signal." Furthermore, the *Fergusson* patent fails to teach the use of "a control board integrating the input interface, the scaler module and the micro-processing device." As a result, it is Applicants' belief that claim 1 is allowable over the *Nakano* et al. and *Fergusson* patents, whether considered individually or in combination.

Insofar as claims 2-10 depend from claim 1, it is Applicants' belief that these claims are also allowable.

In view of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested.

However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

Respectfully submitted,

Dated: April 1, 2003

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EXPRESS MAIL CERTIFICATE

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PATENT TRADEMARK OFFICE

Docket No.: 3158/0I189



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: S.K. LIN et al.

| | | | |
|---|---|---|---|
| Serial No.: | 09/764,750 | Art Unit: | 2674 |
| Confirmation No.: | 7989 | | |
| Filed: | January 18, 2001 | Examiner: | NGUYEN, Jennifer T. |
| For: | LCD MONITOR | | |

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**MARK-UP FOR AMENDMENT OF APRIL 1, 2003**
**PURSUANT TO 37 C.F.R. §1.121**

**Box FEE**
Assistant Commissioner of Patents
Washington, DC 20231

Sir:

**IN THE CLAIMS:**

1. (Amended) A LCD monitor, comprising:

[A] a panel module having a gate driver and a source driver;

[A] a control board disposed on a first side of the panel module, comprising:

[An] an input interface for receiving plural types of video signals, adapted to select a first-type video signal from the plural types of video signals and generate a first digital video signal according to the first-type video signal;

[A] a scaler module, comprising a time control unit, and is provided to receive the first digital video signal; and

[A] a micro-processing device, adapted to output a first control signal that controls the scaler module to generate a gate/source-driving signal for the gate driver and the source driver according to the first digital video signal;

[A] a frame structure, covering the periphery of the panel module; and

[A] a cover structure conjugating the frame structure in the aspect of the first side, and covering upon the first side of the panel module and the control board thereon.

Respectfully submitted,

Dated: April 1, 2003

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